upon their being determined to have reached desired [ones of said at least two] threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired [ones of said at least two] threshold level ranges.

2~~64~~. (Twice Amended) The method of claim 1~~63~~, wherein there are exactly two [of said defined] threshold level ranges.

3~~65~~. (Twice Amended) The method of claim 1~~63~~, wherein there are more than two [of said defined] threshold level ranges.

4~~66~~. (Twice Amended) The method of claim 1~~63~~, wherein [said at least two] the threshold level ranges are separated by exactly one breakpoint threshold level, thereby to provide exactly two non-overlapping threshold level ranges.

5~~67~~. (Twice Amended) The method of claim 1~~63~~, wherein [said at least two] the threshold level ranges are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping threshold level ranges.

6~~68~~. (Twice Amended) The method of claim 1~~63~~, wherein said [at least two defined] desired threshold level ranges include an erased threshold level range.

7~~69~~. (Twice Amended) The method of claim 1~~63~~, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within a selected one of the blocks are changed together to a single given threshold level range prior to applying said appropriate voltage conditions in parallel to the plurality of cells within said one block.

8~~70~~. (Twice Amended) The method of claim 7~~69~~, wherein individual ones of said blocks include a specific number of memory cells and said plurality of memory cells to which said appropriate voltage conditions are applied in parallel are less than [a] said specific number [of memory cells within individual ones of said blocks], and additionally comprising repeating for another plurality of cells within said one block said applying, determining and terminating operations.

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9 71. (Amended) The method of claim 69, 7 wherein individual ones of the blocks of cells contain a number of spare cells [to which the appropriate voltage levels are not normally applied], and further wherein the spare cells within a particular block are substituted in place of any defective cells within said plurality of cells of said particular block.

11 73. (Amended) The method of claim 63, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within individual ones of the blocks are changed together to a single given threshold level range prior to applying said appropriate voltage conditions in parallel to the plurality of cells within one of the blocks, the method further comprising simultaneously changing the threshold levels of cells [of] within a selected two or more blocks to said given level range.

74. (Amended) The method of either of claims 70 or 73, wherein said single given threshold level range is within one of ~~said at least two defined threshold level [regions] ranges~~.

12 75. (Amended) The method of claim 63 wherein the desired ones of [at least two] said threshold level ranges reached by applying appropriate voltage conditions to the plurality of memory cells correspond to a chunk of input data being programmed into the memory system.

13 76. (Amended) The method of claim 12 75, wherein the plurality of cells are determined to have reached the desired [ones of said at least two] threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of input data.

14 77. (Amended) The method of claim 13 76, wherein the chunk of input data is stored in a cache memory prior to being programmed into [the] memory [system] cells within the EEprom.

16 78. (Amended) The method of either of claims 365 or 367, wherein terminating the application of appropriate voltage conditions to individual ones of the plurality of memory cells occurs upon their being determined to have been programmed to

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within the desired [ones of said at least two] threshold levels by a margin.

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~~1881~~. (Amended) The method of either of claims ~~3,65~~ or ~~5,67~~, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with two or more reference levels stored in two or more of the memory cells.

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~~3295~~. (Amended) A method of storing [a chunk] multiple bits of binary data in [an array of integrated circuit] a chunk of non-volatile memory cells which individually have more than two programmable states, comprising:

[addressing a plurality of said memory cells sufficient in number to store the chunk of binary data,]

applying electrical programming parameters in parallel to [the addressed] cells within said chunk,

monitoring the states [in which] of individual [the addressed] cells [are individually programmed] within said chunk, and

terminating application of programming parameters to individual [ones of said addressed] cells within said chunk when they are monitored to have reached desired ones of said more than two programmable states corresponding to the [chunk] multiple bits of data being stored, while continuing to apply said programming parameters to others of the [addressed] cells within said chunk, until all of the [addressed] cells within said chunk are determined to have reached their programmable states corresponding to the [chunk] multiple bits of data being stored.

~~3396~~. (Amended) The method of claim ~~95~~ 32, wherein, prior to applying electrical programming parameters to [the addressed] cells within said chunk, at least the [addressed] cells within said chunk are all reset to a common state different than [either] any of said more than two programmable states.

~~3497~~. (Amended) The method of claim ~~95~~ 32, wherein, prior to applying electrical programming parameters to the [addressed] cells

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